LISTING OF THE CLAIMS

A listing of all claims and their current status in accordance with 37 C.F.R. § 1.121(c) is provided below.

1. (original) A system comprising:

a processor; and

a memory device coupled to the processor that comprises:

a first voltage bus;

a second voltage bus; and

a bridge circuit coupled between the first voltage bus and the second voltage bus, wherein the bridge circuit is adapted to:

receive an input signal;

connect the first voltage bus and the second voltage bus together if the input signal is a first control signal; and

isolate the first voltage bus from the second voltage bus if the input signal is a second control signal.

2. (original) The system, as set forth in claim 1, wherein the memory device comprises a dynamic random access memory (DRAM) device.

3. (original) The system, as set forth in claim 1, wherein the memory device comprises a static random access memory (SRAM) device.

4. (original) The system, as set forth in claim 1, wherein the processor is coupled to a communication port to communicate with an input/output device.

5. (original) The system, as set forth in claim 1, wherein the processor is coupled to a user interface.

6. (original) The system, as set forth in claim 1, wherein the processor is coupled to a display to present information to a user.

7. (original) The system, as set forth in claim 1, wherein the first voltage bus is a voltage supply bus for periphery circuitry and the second voltage bus is a voltage supply bus for array circuitry.

8. (original) The system, as set forth in claim 1, wherein the processor is coupled to a power supply that is external to the memory device.

9. (original) The system, as set forth in claim 8, comprising a plurality of power amplifiers coupled to the first voltage bus and adapted to:

receive power from a power supply; and

apply a voltage to the first voltage bus.

10. (original) The memory device, as set forth in claim 8, comprising at least one standby amplifier coupled to one of the first voltage bus and the second voltage bus and adapted to supply power to the one of the first voltage bus and the second voltage bus.

11. (original) The system, as set forth in claim 8, comprising at least one voltage detector coupled to one of the first voltage bus and the second voltage bus and adapted to determine the voltage on the one of the first voltage bus and the second voltage bus.

12. (original) The system, as set forth in claim 11, wherein the at least one voltage detector generates the first control signal that is a power-up control signal.

13. (original) The system, as set forth in claim 1, wherein the processor generates the second control signal that is an activation signal.

14. (original) The system, as set forth in claim 1, wherein the bridge circuit comprises:

a first input of a NAND gate coupled to a voltage detector;

a first inverter coupled between a second input of the NAND gate and an output of a regulator control;

a second inverter coupled between the output of the NAND gate and a gate of a transistor; and

a source of the transistor coupled to the first voltage bus and a drain of the transistor to the second voltage bus.

15. (original) A memory device comprising:

a periphery voltage bus coupled to periphery circuitry;

an array voltage bus coupled to array circuitry; and

a bridge circuit coupled between the periphery voltage bus and the array voltage bus, wherein the bridge circuit is configured to:

receive an input signal;

connect the periphery voltage bus and the array voltage bus together if the input signal is a first control signal; and

isolate the periphery voltage bus from the array voltage bus if the input signal is a second control signal.

16. (original) The memory device, as set forth in claim 15, wherein the memory device comprises a dynamic random access memory (DRAM) device.

17. (original) The memory device, as set forth in claim 15, wherein the memory device comprises a static random access memory (SRAM) device

18. (original) The memory device, as set forth in claim 15, comprising a plurality of power amplifiers coupled to the periphery voltage bus and adapted to receive power being generated by a device external to the memory device.

19. (original) The memory device, as set forth in claim 15, comprising a plurality of standby amplifiers coupled to one of the periphery voltage bus and the array voltage bus, wherein the plurality of standby amplifiers supplies power to periphery circuitry and the array circuitry.

20. (original) The memory device, as set forth in claim 15, comprising at least one voltage detector coupled to one of the periphery voltage bus and the array voltage bus, wherein the at least one voltage detector is adapted to determine the voltage on one of the periphery voltage bus and the array voltage bus.

21. (original) The memory device, as set forth in claim 15, wherein the first control signal comprises a power-up control signal.

22. (original) The memory device, as set forth in claim 15, wherein the first control signal comprises a standby control signal.

23. (original) The memory device, as set forth in claim 15, wherein the second control signal comprises an activation control signal.

24. (original) A method of operating a device comprising the acts of:

providing a first voltage to a periphery voltage bus and a second voltage to an array voltage bus;

receiving a control signal at a bridge circuit;

determining if the control signal indicates one of a first condition and a second condition;

coupling the periphery voltage bus to the array voltage bus if the control signal indicates the first condition; and

isolating the periphery voltage bus from the array voltage bus if the control signal indicates the second condition.

25. (original) The method, as set forth in claim 24, wherein the periphery voltage bus reaches the first voltage in a first time period and the array voltage bus reaches the second voltage in a second time period when the periphery voltage bus is isolated from the array voltage bus, wherein the first time period is different from the second time period.

26. (original) The method, as set forth in claim 24, wherein the periphery voltage bus reaches the first voltage in a third time period and the array voltage bus reaches the second voltage in the third time period, when the periphery voltage bus and the array voltage bus are coupled together, wherein the third time period is different than each of the first time period and the second time period.

27. (original) The method, as set forth in claim 26, wherein the third time period is greater than or equal to one of the first and second time periods and less than or equal to another of the first and second time periods.

28. (original) The method, as set forth in claim 24, comprising determining if the control signal is a power down control signal.

29. (original) The method, as set forth in claim 24, wherein the second condition comprises an activation signal.

30. (original) The method, as set forth in claim 24, wherein the first condition comprises a power-up signal.

31. (original) The method, as set forth in claim 24, comprising supplying the first voltage and the second voltage from a plurality of standby amplifiers attached to one of the periphery voltage bus and the array voltage bus.

32. (original) The method, as set forth in claim 24, comprising monitoring the first voltage and the second voltage from a voltage detector coupled to one of the periphery voltage bus and the array voltage bus.

33. (original) A method of manufacturing a memory device comprising the acts of: providing a memory device having a first voltage bus and a second voltage bus;

coupling a power amplifier to one of the first voltage bus and the second voltage bus;

coupling a bridge circuit to the first voltage bus and the second voltage bus;

encoding the memory device to provide a first control signal that couples the first voltage bus to the second voltage bus in response to a first condition; and

encoding the memory device to provide a second control signal that isolates the first voltage bus from the second voltage bus in response to a second condition.

34. (original) The method, as set forth in claim 33, comprising coupling a voltage detector to one of the first voltage bus and the second voltage bus.

35. (original) The method, as set forth in claim 34, comprising encoding the voltage detector to measure voltage on one of the first voltage bus and the second voltage bus.

36. (original) The method, as set forth in claim 33, comprising coupling a regulator control to the bridge circuit, wherein the regulator control is configured to deliver one of the one of the first control signal and the second control signal to the bridge circuit.

37. (original) The method, as set forth in claim 36, wherein in the bridge circuit comprises:

coupling a first input of a NAND gate to a voltage detector;

coupling a first inverter between a second input of the NAND gate and an output of the regulator control;

coupling a second inverter between the output of the NAND gate and a gate of a transistor; and

coupling a source of the transistor to the first voltage bus and a drain of the transistor to the second voltage bus.

38. (original) The method, as set forth in claim 33, comprising coupling a standby amplifier to one of the first voltage bus and the second voltage bus to provide power to the first and second voltage buses.

39. (original) The method, as set forth in claim 33, comprising coupling periphery circuitry to the first voltage bus.

40. (original) The method, as set forth in claim 33, comprising coupling array circuitry to the second voltage bus.